CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A vertical field effect transistor including

a semiconductor pillar conduction channel,

gate electrodes in trenches adjacent said semiconductor pillar,

a layer of insulator adjacent said gate electrodes and opposite said semiconductor pillar,

sidewalls adjacent said semiconductor pillar above said gate electrodes in said trenches,

insulator material in said trenches above said gate electrodes and adjacent said sidewalls, said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar.

2. A vertical transistor as recited in claim 1, further including isolation material adjacent said layer of insulating material and surrounding said vertical transistor, said isolation material being selectively etchable relative to said layer of insulator.

3. A vertical transistor as recited in claim 2, further including

a contact formed in an opening in said isolation material adjacent said insulating material to a conductive region at an end of said pillar.

4. A vertical transistor as recited in claim 1, further including

a contact formed in an opening to an end of said pillar, and

a contact formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall on said pillar.

5. A vertical transistor as recited in claim 1, further including

a spacer in said trench between said gate structure and a bottom of said trench.

6. An integrated circuit device including

isolation material surrounding transistor locations in a substrate,

vertical field effect transistors formed at said transistor locations and having a gate electrode structure formed in a trench,

a layer of insulator material in said trenches between said isolation material and said gate electrode structure, said isolation material being selectively etchable relative to said layer of insulator and

a contact opening formed along an interface of said layer of insulator material and said isolation material.

7. A device as recited in claim 6, wherein said gate structure includes dual gate electrodes extending on opposite sides of a conduction channel.

8. A device as recited in claim 6, further including

a contact formed in said contact opening in said isolation material adjacent said insulating material and extending to a conductive region extending below said pillar.

9. A device as recited in claim 6, further including

a contact formed in an opening to an end of said pillar, and

a contact formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall on said pillar.

10. A device as recited in claim 61, further including

a spacer in said trench between said gate structure and a bottom of said trench.

11. A method of making a semiconductor device including a field effect transistor, said method including steps of

forming a semiconductor pillar in a trench in a body of a first insulating material, said trench extending to a layer of semiconductor material,

forming a layer of a second insulating material on walls of said trench, and

etching a contact opening to said semiconductor material through said first insulating material selectively and adjacent to said second insulating material.

12. A method as recited in claim 11, including further steps of

forming a gate structure adjacent sides of said pillar,

forming layers and/or sidewalls of selectively etchable materials over said gate structure and said pillar, and

forming contact openings to an end of said pillar and said gate structure by selective etching of said layers at locations above and adjacent said pillar, respectively.

13. A method as recited in claim 11, including further steps of

defining a height of said pillar by thickness of a layer of sacrificial material.

14. A method as recited in claim 13, wherein said sacrificial material is germanium oxide.

15. A method as recited in claim 11, wherein said step of forming said pillar is performed by epitaxial semiconductor growth in a trench.

16. A method as recited in claim 11, wherein said step of forming said pillar is performed by etching of a layer of semiconductor material.

17. A method as recited in claim 11, including a further step of

limiting a dimension of said pillar by a distance between isolation structures.

18. A transistor comprising

a substrate,

a first diffusion,

a second diffusion above said first diffusion,

a channel extending vertically between said first diffusion and said second diffusion,

a gate structure extending on at least one side of said channel, and

a contact to said first diffusion borderless to said gate structure.

19. A transistor as recited in claim 18, wherein said transistor is a vertical transistor and wherein said first diffusion is formed in said substrate and said second diffusion is formed on the channel.

20. A transistor as recited in claim 18, wherein said gate extends on two sides of said channel.

21. A transistor as recited in claim 19, wherein a contact to said gate extends above and on two sides of said second diffusion.

22. A transistor as recited in claim 19, further including separate contacts to separate portions of said gate structure on different sides of said channel.

23. A transistor as recited in claim 18, wherein said gate structure extends on at least three sides of said channel.

24. A transistor as recited in claim 18, further including a contact to said second diffusion borderless to said gate structure.

25. A transistor as recited in claim 18, wherein said transistor comprises a pillar of single crystal silicon having an edge.

26. A transistor as recited in claim 25, wherein said pillar comprises said first diffusion, said channel and said second diffusion, said gate structure extending adjacent said pillar.

27. A transistor as recited in claim 26, wherein said first diffusion extends into single crystal silicon beneath said pillar and extends below said gate structure for formation of a contact adjacent said gate structure.

28. A transistor as recited in claim 26, further comprising

an insulator adjacent said gate structure, wherein said contact to said first diffusion comprises a conductive layer adjacent said insulator.

29. A transistor as recited in claim 26, wherein said gate structure is borderless to said second diffusion.

30. A transistor as recited in claim 26, wherein said contact to said second diffusion comprises a spacer self-aligned to said edge.

31. A transistor as recited in claim 26, wherein said pillar extends above said gate structure.

32. A transistor as recited in claim 18, further comprising

an isolation structure, wherein said transistor is self-aligned to said isolation structure.

33. A transistor as recited in claim 18, further comprising

a contact between said first diffusion and another diffusion forming part of a second transistor, wherein said contact between said first diffusion and said another diffusion extends over insulation between said first transistor and said second transistor.

34. A transistor as recited in claim 33, wherein said insulation comprises an etched and deposited isolation structure.

35. A transistor as recited in claim 32 wherein said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation.

36. A transistor as recited in claim 33, wherein said first transistor and said second transistor comprise an inverter and wherein said contact to said first diffusion is a contact to said inverter.

37. A transistor as recited in claim 18, wherein said gate structure comprises a continuous interior wall entirely surrounding said channel and spaced therefrom by a dielectric layer.

38. A transistor as recited in claim 18 wherein said gate structure is self-aligned to said channel.

39. A transistor as recited in claim 18 wherein said first diffusion comprises a dopant species provided separately from said second diffusion.

40. A transistor as recited in claim 18, wherein said channel is of sub-lithographic width.

41. A transistor as recited in claim 18, wherein said first diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a first diffusion contact formed in the opening.

42. A transistor as recited in claim 18, wherein said second diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a second diffusion contact formed in the opening.

43. A transistor as recited in claim 18, wherein said gate structure includes

top, bottom and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a gate contact formed in the opening.

44. A transistor as recited in claim 18, wherein said first diffusion, said second diffusion and said gate structure each include a borderless contact.